AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1-85. (Cancelled)

86. (New) A servo controller interface for a disk controller, wherein the disk controller includes a servo controller, the servo controller interface comprising:

a first interface configured to communicate with a first processor over a first bus in a first frequency domain;

a second interface configured to communicate with a second processor over a second bus in a second frequency domain that is different than the first frequency domain;

a speed matching first in first out (FIFO) memory module configured to

receive first data from the first processor over the first bus via the first interface in the first frequency domain, and

receive second data from the second processor over the second bus via the second interface in the second frequency domain; and

a pipeline control module configured to

select which of the first data and the second data is transmitted to the speed matching FIFO memory module in response to no conflicts existing between the first processor and the second processor, and

selectively insert wait cycles during transmission of one of the first data and the second data in response to a conflict existing between the first processor and the second processor.

87. (New) The servo controller interface of claim 86, wherein the servo controller interface operates in the first frequency domain, and the servo controller operates in one of the first frequency domain and a third frequency domain.

88. (New) The servo controller interface of claim 86, wherein the first processor and the second processor share memory mapped registers within the servo controller.

89. (New) The servo controller interface of claim 86, wherein the pipeline control module determines a number of the wait cycles to insert based on the first frequency domain.

90. (New) The servo controller interface of claim 86, wherein the pipeline control module selectively inserts the wait cycles

based on whether the transmission corresponds to a read access or a write access.

91. (New) The servo controller interface of claim 86, wherein the pipeline control module inserts the wait cycles during a read access in response to a conflict existing between the first processor and the second processor.

92. (New) The servo controller interface of claim 86, wherein the pipeline control module de-asserts a ready signal during a write access in response to a conflict existing between the first processor and the second processor.

93. (New) The servo controller interface of claim 86, wherein:

in response to a conflict existing between the first processor and the second processor, the pipeline control module (i) inserts the wait cycles for the first data and (ii) does not insert the wait cycles for the second data; and

the first frequency domain has a higher frequency than the second frequency domain.

94. (New) A method of operating a servo controller interface for a disk controller, wherein the disk controller includes a servo controller, the method comprising:

communicating with a first processor over a first bus in a first frequency domain using a first interface;

communicating with a second processor over a second bus in a second frequency domain that is different than the first frequency domain using a second interface;

receiving first data at a speed matching first in first out (FIFO) memory module from the first processor over the first bus via the first interface in the first frequency domain;

receiving second data at the speed matching FIFO memory module from the second processor over the second bus via the second interface in the second frequency domain;

selecting which of the first data and the second data is transmitted to the speed matching FIFO memory module in response to no conflicts existing between the first processor and the second processor; and

selectively inserting wait cycles during transmission of one of the first data and the second data in response to a conflict existing between the first processor and the second processor.

95. (New) The method of claim 94, wherein the servo controller interface operates in the first frequency domain, and the servo controller operates in one of the first frequency domain and a third frequency domain.

96. (New) The method of claim 94, wherein the first processor and the second processor share memory mapped registers within the servo controller.

97. (New) The method of claim 94, further comprising determining a number of the wait cycles to insert based on the first frequency domain.

98. (New) The method of claim 94, further comprising selectively inserting the wait cycles based on whether the transmission corresponds to a read access or a write access.

99. (New) The method of claim 94, further comprising inserting the wait cycles during a read access in response to a conflict existing between the first processor and the second processor.

100. (New) The method of claim 94, further comprising de-asserting a ready signal during a write access in response to a conflict existing between the first processor and the second processor.

101. (New) The method of claim 94, further comprising, in response to (i) a conflict existing between the first processor

and the second processor and (ii) the first frequency domain having a greater frequency than the second frequency domain:

inserting the wait cycles for the first data; and

not inserting the wait cycles for the second data.